IN THE SPECIFICATION

Please amend paragraph [00072] as follows:

[00072] Referring now to FIG. 5, FIG. 5 depicts determinant calculation 400 of a sub-matrix in accordance with one embodiment of the present invention. As illustrated, the depiction represents the vector element pairs (rows) of the sub-matrices stored within 128-bit double-precision floating-point registers 209, or 64-bit single-precision register 215. However, those skilled in the art will recognize that the present invention may be implemented with the desired registers available from an architecture, such that registers containing less than 64 bits may be utilized, while sacrificing precision provided by ~~doublepoint~~ double-precision representation of floating-point values.

Please amend paragraph [00075] as follows:

[00075] As illustrated by FIG. 5, as well FIGS. 6-11, the various selections of registers to be loaded during the various calculations as will be described herein, is provided to illustrate one possible embodiment of the invention. However, those skilled in the art will recognize that the various selection of registers in which to load and when to copy-in or replace the element from memory may be provided via compiler optimizations in the generated assembly code when the present invention is implemented in software. Alternatively, the various registers are selected in implementations using application specific integrated circuits or microcode for directing integrated circuit packet implementations of the ~~present invention~~embodiments described herein.

Please amend paragraph [000105] as follows:

[000105] Accordingly, as ~~described herein~~ in one embodiment, the calculation of the inverse of a source matrix is performed by sub-dividing the source matrix into four sub-matrices. This enables storage of each of the rows of a sub-matrix within a single SIMD register. As such, concurrent calculation of the various matrix products, determinants, scaling and residue provides improved efficiency when calculating the inverse of a source matrix. This follows due to the fact that the inverse of each sub-matrix is recombined to form the inverse of the source matrix 300 in accordance with Equation 16.

Please amend paragraph [000114] as follows:

[000114] Several ~~aspects of one implementation~~embodiments of the matrix inversion process for providing vector transformations have been described. However, various implementations of the matrix inversion process provide numerous features including, complementing, supplementing, and/or replacing the features described above. Features can be implemented as part of an ALU, a programmed device, or as part of a software library in different implementations. In addition, the

foregoing ~~description~~embodiments, for purposes of explanation, used specific nomenclature to provide a thorough understanding of the invention. However, it will be apparent to one skilled in the art that the specific details are not required in order to practice the ~~invention~~embodiments described herein.

Please amend paragraph [000116] as follows:

[000116] It is to be understood that even though numerous characteristics and advantages of various embodiments ~~of the present invention~~ have been set forth in the foregoing description, together with details of the structure and function of various embodiments of the invention, this disclosure is illustrative only. In some cases, certain subassemblies are only described in detail with one such embodiment. Nevertheless, it is recognized and intended that such subassemblies may be used in other embodiments of the invention. Changes may be made in detail, especially matters of structure and management of parts within the principles of the present invention to the full extent indicated by the broad general meaning of the terms in which the appended claims are expressed.

Please amend paragraph [000117] by deleting it in entirety as follows:

~~**[000117]** The present invention provides many advantages over known techniques. The present invention includes the ability to provide improved computation locality. As a result, faster computation of a matrix inverse is achieved in environments with a limited number of registers. Moreover, the matrix inversion process benefits from architectures that support two element SIMD vectors, such that parallel calculation is supported when using two element double vectors.~~